IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Jeff W. Hall, et al.

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Examiner: L. Nguyen

Title: LOW VOLTAGE OUTPUT DRIVE CIRCUIT

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BY: _____*Lydia McNamara*_____   DATE: _____MARCH 1, 2002_____
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SIR:

PRELIMINARY AMENDMENT

This preliminary amendment is filed in conjunction with a continuation in part (CIP) application filed pursuant to Rule 1.53(b) of copending Application No. 09/580,560 filed May 30, 2001. The entire specification, including claims, figures and drawings, of prior filed patent Application No. 09/580,560 is included herewith. Please include the entire content of Application No. 09/580,560, which is incorporated by reference herein, as the basis for the CIP application along with the application supplements provided within this preliminary amendment.

IN THE DRAWINGS

Please add FIGs. 7-9 filed concurrently with this preliminary amendment.

IN THE ABSTRACT

Please delete the ABSTRACT and replace it with the following.

--An amplifier (170) includes first and second depletion mode transistors (161, 162) operating in response to first and second complementary signals (V_{AMP+}, V_{AMP-}), respectively, which route a first current (I_{STACK1}) from a first supply terminal (171) to an output (169) of the amplifier. Third and fourth depletion mode transistors (163, 164) receive the first and second complementary signals to route a second current (I_{STACK2}) from a second supply terminal (Ground) to the output. The first and second currents are summed to produce an output signal (V_{AMP2}).--

IN THE SPECIFICATION

Please add the following sentence as the first paragraph following the title.

--The present application is based on prior U.S. application No. 09/580,560, filed on May 30, 2000, which is hereby incorporated by reference, and priority thereto for common subject matter is hereby claimed.--

Please change the title from "LOW VOLTAGE OUTPUT DRIVE CIRCUIT" to "LOW VOLTAGE AMPLIFYING CIRCUIT".

Please delete the text from page 1, line 6, through page 3, line 30 and replace with the following.

--The present invention relates in general to electronic circuits and, more particularly, to amplifying circuits that operate at low supply voltage levels.

As integrated circuits achieve higher levels of integration, there is a corresponding need to operate the circuits at reduced voltage levels in order to maintain power dissipation at manageable levels. For example, it is anticipated that future microprocessors and other digital circuits will need to operate with power supply voltages of 0.5 volts to maintain an acceptable die temperature. Future circuits are expected to operate with even lower supply voltages.

A low supply voltage typically is produced by a voltage regulator implemented as an integrated circuit. The regulator includes an error amplifier to sense the supply voltage and feed back an error signal that adjusts the voltage level to maintain regulation. The error amplifier and its associated circuitry preferably also operate at a low voltage in order to achieve a low power dissipation by the regulator circuit.

Most if not all integrated circuit amplifiers operate only at supply voltages that exceed the conduction threshold of the integrated circuit's transistors. When the supply voltage drops below the conduction threshold level, the transistors cease to function and gain of the amplifiers drops quickly to zero. In a case where the amplifier is being used in a voltage regulator, the rapid loss of gain can cause the regulator's output voltage to transition out of its specified range, which can damage both the regulator and the circuits operating from the regulator's output supply voltage.

Accordingly, there is a need for an amplifier circuit and method of amplifying that maintains functionality at lower

supply voltages than what is currently available.—

Please remove the paragraph from page 4, lines 4-15 and replace with the following.

--FIG. 1 is a block diagram of a supervisor circuit and microprocessor;

FIG. 2 is a waveform plot of an output signal of a prior art supervisor circuit;

FIG. 3 is a waveform plot of an output signal of a supervisor circuit;

FIG. 4 is a schematic diagram of a trigger circuit of the supervisor circuit;

FIG. 5 is a block diagram of a prior art linear regulator circuit;

FIG. 6 is a block diagram of a first regulator circuit;

FIG. 7 is a schematic diagram of a second regulator circuit including an amplifier;

FIG. 8 is a schematic diagram of the amplifier; and

FIG. 9 is a schematic diagram of an alternate embodiment of the amplifier.—

Please insert the following text after page 12, line 17.

--In the following figures, elements having the same reference numbers have similar functionality.

FIG. 7 is a schematic diagram of a voltage regulator 100, including an amplifier 102, transistors 104 and 106, resistors 108 and 110 and capacitors 112 and 114. Voltage regulator 100 receives an input supply voltage V_{SUPP} on a supply terminal coupled to a node 118 and produces a regulated voltage V_{REG} at an output 120. Regulator 100 is suitable for integrating on a semiconductor die to form an integrated voltage regulator circuit.

Resistors 108 and 110 are scaled to a predetermined ratio

and serially coupled between output 120 and ground potential
to function as a voltage divider that monitors or senses
regulated voltage V_{REG} and provides a divided sense voltage
V_{SENSE} on a node 122.

Amplifier 102 comprises a differential input-differential
output voltage or transconductance amplifier configured to
operate from supply voltage V_{SUPP} at values approaching zero
volts. In one embodiment, $V_{SUPP}=0.3$ volts. An inverting input
is coupled to node 122 to receive sense voltage V_{SENSE} and a
non-inverting input at a node 124 receives a reference voltage
V_{REF1}. An error voltage $V_{ERR}=(V_{REF1}-V_{SENSE})$ applied across the
inverting and non-inverting inputs is amplified to produce a
differential output signal $V_{AMP}=(V_{AMP+}-V_{AMP-})$ across output nodes
128 and 126, where V_{AMP-} and V_{AMP+} are the component signals of
V_{AMP} and have opposing phases.

The transient characteristics of amplifier 102 are a
function of the impedances of nodes 126 and 128, which are
determined by loop stabilization capacitors 112 and 114 and
the gate capacitances of transistors 104 and 106, and
therefore are highly capacitive. Accordingly, the output
stage of amplifier 102 is configured to drive nodes 126 and
128 with currents high enough to meet specified transient
response characteristics and low enough to ensure loop
stability under the specified operating and environmental
conditions of regulator 100.

Transistors 104 and 106 are formed as metal oxide
semiconductor field effect transistors (MOSFET) operating in
the depletion mode. Transistor 104 is an n-channel MOSFET
while transistor 106 is a p-channel MOSFET as shown in FIG. 7.
Transistors 104 and 106 are serially coupled between input
120 and output 118, with their sources being commonly coupled
to a node 127 to function as a pass element of regulator 100.
Because transistors 104 and 106 are formed as series coupled
depletion mode devices, their conduction thresholds are   ·
negative, so they are conductive even with zero volts of gate

to source bias potential. As a result, regulator 100 is able
to maintain regulation when the input-output voltage
differential ($V_{SUPP}-V_{REG}$) approaches zero volts. In one
embodiment, input-output voltage differential ($V_{SUPP}-V_{REG}$) is 0.2
volts. In one embodiment, transistors 104 and 106 are formed
to have typical conduction thresholds of -0.2 volts, thereby
providing conduction at zero volts of gate to source
potential.

In operation, assume that V_{SUPP}=0.3 volts, V_{REF1}=0.125 volts
and V_{REG} initially is zero, with a target value of 0.25 volts.
Further assume that the resistances of resistors 108 and 110
are equal, so V_{SENSE}=V_{REG}/2. Since V_{REG} is zero, V_{SENSE} is zero as
well, and therefore less than V_{REF1}, so V_{AMP-} decreases while
V_{AMP+} increases, turning on transistors 104 and 106 to couple a
current I_{LOAD} from input 118 to output 120 to charge an external
load capacitor 130 to increase the value of V_{REG}. I_{LOAD}
continues to flow until V_{REG} reaches its target value of 0.25
volts, at which time V_{SENSE}=V_{REF1}=0.125 volts, approximately.
While V_{REG} is at its target value, amplifier 102 controls the
conduction of transistors 104 and 106 such that I_{LOAD} flows at a
level sufficient to supply the current requirements of the
load circuitry (not shown) operating from V_{REG}, thereby
maintaining regulation. In one embodiment, regulator 100 is
configured to supply I_{LOAD} to a magnitude of one hundred
milliamperes.

Under normal conditions V_{REG} does not exceed its target
value, but load switching or system noise may result in
momentarily increasing V_{REG} to a value greater than the 0.25
volt target value. If that occurs, amplifier 102 produces
values of V_{AMP+} and V_{AMP-} that reduce the conduction of
transistors 104 and 106 to allow the flow of current to the
load circuitry to be supplied from charge stored on capacitor
130 until V_{REG} decays to its target value.

FIG. 8 shows a schematic diagram of amplifier 102 in
further detail, including depletion mode MOSFETs 140-144.

Transistor 140 is an n-channel device whose gate and
source operate at ground potential to function as a current
source that supplies a bias current I_{BIAS} to a common node 145.
Transistors 143-144 are p-channel devices whose sources and
gates are coupled to node 118 to function as current sources
or high impedance loads that provide amplifier 102 with a high
open loop gain. Alternatively, high impedance resistors or
other types of devices can be used to perform functions
equivalent to those performed by transistors 140 and 143-144.
However, such alternative devices have the disadvantage of
consuming a larger area of a semiconductor die, and therefore
have a higher cost, than transistors 140 and 143-144.

Transistors 141-142 are configured as a differential pair
receiving V_{SENSE} and V_{REF1} as a differential input signal that
routes I_{BIAS} through transistors 143 and 144 to produce
component differential signals V_{AMP+} and V_{AMP-} of differential
output signal V_{AMP}. Nodes 126 and 128 are relatively high
impedance nodes which allow amplifier 102 to be easily
compensated by capacitors 112 and 114 (shown in FIG. 7) when
operated in a closed loop condition such as that of regulator
100.

The use of depletion mode devices for transistors 140-144
maintains their conduction and allows amplifier 102 to
function at values of supply voltage V_{SUPP} that approach zero.
Accordingly, amplifier 102 is well suited for low voltage
applications such as in regulating the supply voltage of a low
voltage microprocessor. Although amplifier 102 is shown and
described as being used as an active component of voltage
regulator 100, it is evident that amplifier 102 is suitable
for use in virtually any other analog application that would
benefit from its economical structure and low voltage
operation.

FIG. 9 shows a schematic diagram of an amplifier 170
receiving oppositely phased differential input signals V_{IN+} and
V_{IN-} and producing a single ended amplified output signal V_{AMP2}

at an output 169. Amplifier 170 is coupled to a supply
terminal 118 to operate from a supply voltage V_{SUPP}. Amplifier
170 includes depletion mode MOSFET transistors 140-144 and
161-164 and a level shift circuit 133, and is suitable for use
as a low voltage amplifier in an analog amplification
application such as an error amplifier in a voltage regulator.
In an alternate embodiment, amplifier 170 is configured with
a high transconductance or voltage gain for use as a
comparator.

Transistors 140-144 function as a first or input stage of
amplifier 170 and operate in a fashion similar to that
described in the description of FIG. 8. Consequently, the
first stage has the benefit of operating at values of V_{SUPP} that
approach zero.

Level shifter 133 level shifts component differential
signals V_{AMP+} and V_{AMP-} to produce level shifted signals V_{LS+} and
V_{LS-} on node 131 and 129, respectively. V_{LS+} and V_{LS-} retain the
information contained in V_{AMP+} and V_{AMP-} but are level shifted by
a DC voltage in order to bias transistors 161-164 for the
desired operation. For example, if class A operation is
desired, the level shifting DC voltage may be set to one-half
the value of supply voltage V_{SUPP}. Other level shifting
voltages may be used to provide other classes of operation.

Transistors 161-164 function as a second or output stage
of amplifier 170 whose operation is described as follows.
Transistor 161 is an n-channel device controlled by component
signal V_{LS-} to set the conduction between supply terminal 118
and a node 166. Transistor 162 is a p-channel device
controlled by component signal V_{LS+} to set the conduction
between node 166 and output 169. The conduction of
transistors 161-162 determine the level of a current I_{STACK1}
that is routed from supply terminal 118 to output 169 as a
first component of output signal V_{AMP2}.

Transistor 164 is a p-channel device controlled by
component signal V_{LS-} to set the conduction between ground

potential and a node 168. Transistor 163 is an n-channel
device controlled by component signal V_{AMP+} to set the
conduction between node 168 and output 169. The conduction of
transistors 163-164 determines the level of a current I_{STACK2}
that is routed from ground to output 169 as a second component
of output signal V_{AMP2}.

Output voltage V_{AMP2} is developed from an output current
I_{OUT} that flows from output 169 to a load 180 as the difference
between currents I_{STACK1} and I_{STACK2}.

It can be seen that the present invention provides an
amplifier that occupies a small die area and has a low cost
while operating with an input-output voltage differential
approaching zero volts. First and second depletion mode
transistors operate in response to first and second signals,
respectively, to route a first current from a first supply
terminal to an output of the amplifier. Third and fourth
depletion mode transistors operate in response to the first
and second signals to route a second current from a second
supply terminal to the output. The first and second currents
are summed to develop an output signal at the output. The
negative thresholds inherent in depletion mode transistors
ensures active functionality with zero volts gate to source
potential, which allows the amplifier to function at very low
supply voltages, even approaching zero volts. The first or
second signal can be coupled to a reference voltage to operate
the amplifier as a voltage regulator.--

IN THE CLAIMS

Please cancel claims 1-22, which were elected in parent application 09/580,560 pursuant to a restriction requirement under 35 U.S.C. § 121 dated April 9, 2001. Add new claims 27-39 as follows. Claims 23-39 are pending in the application.

27. (New) An amplifier, comprising:

first and second depletion mode transistors operating in response to first and second signals, respectively, for routing a first current from a first supply terminal to an output of the amplifier; and

third and fourth depletion mode transistors operating in response to the first and second signals for routing a second current from a second supply terminal to the output for summing with the first current to produce an output signal.

28. (New) The amplifier of claim 27, wherein the first depletion mode transistor is an n-channel device having a gate that receives the first signal to control a first conduction path between the first supply terminal and a first node of the amplifier, the second depletion mode transistor is a p-channel device having a gate that receives the second signal to control a conduction path between the first node and the output, the third depletion mode transistor is a p-channel device having a gate that receives the first signal to control a conduction path between the second supply terminal and a second node, and the fourth transistor is an n-channel device having a gate that receives the second signal to control a conduction path between the second node and the output.

29. (New) The amplifier of claim 28, wherein the first transistor has a source coupled to the first node and a drain coupled to the first supply terminal, the second transistor

has a source coupled to the first node and a drain coupled to the output, the third transistor has a source coupled to the second node and a drain coupled to the second supply terminal, and the fourth transistor has a source coupled to the second node and a drain coupled to the output.

30. (New) The amplifier of claim 29, further comprising a differential amplifier including:

a first differential transistor having a gate that receives the first signal and a drain coupled to the gates of the first and third depletion mode transistors; and

a second differential transistor having a gate that receives the second signal, a drain coupled to the gates of the second and fourth depletion mode transistors, and a source coupled to a source of the first differential transistor for routing a bias current with the first and second signals.

31. (New) The amplifier of claim 30, wherein the first and second differential transistors are depletion mode devices.

32. (New) The amplifier of claim 30, further comprising a fifth depletion mode transistor having a gate and a source coupled to the second supply terminal and a drain coupled to the source of the second differential transistor for supplying the bias current.

33. (New) An amplifier, comprising:

a gain stage having first and second inputs for receiving a differential input signal and first and second outputs for providing a differential amplified signal; and

an output stage including first and second depletion mode transistors operating in response to the differential amplified signal and serially coupled between a supply terminal and an output of the amplifier for providing an output signal.

34.   (New)   The amplifier of claim 33, further comprising a
feedback path from the output of the amplifier to the first
input of the gain stage to reduce the gain of the amplifier.

35.   (New)   The amplifier of claim 34, wherein the feedback
path includes:
        a first resistor coupled between the output of the
amplifier and the first input of the gain stage; and
        a second resistor coupled from the first input of the
gain stage to a reference node.

36.   (New)   The amplifier of claim 35 for functioning as a
voltage regulator, wherein the differential input signal
includes a reference voltage applied to the second input of
the gain stage to maintain the output signal at a constant
potential.

37.   (New)   The amplifier of claim 36, wherein a difference
between a supply voltage at the supply terminal and the
constant potential of the output signal is less than 0.2
volts.

38.   (New)   The amplifier of claim 33, wherein the first
depletion mode transistor is an n-channel device having a
drain coupled to the supply terminal and a source coupled to a
node, and the second depletion mode transistor is a p-channel
device having a source coupled to the node and a drain coupled
to the output of the amplifier.

39.   (New)   The amplifier of claim 33, further comprising a
level shift circuit having first and second inputs for level
shifting the differential amplified signal by a predefined
potential to provide a differential level shifted signal at
first and second outputs of the level shift circuit.

Formalities

All pending claims are rewritten below in clean form pursuant to Rule 1.121 § (1)(i).

23.   A linear regulator circuit having an input coupled for receiving an input voltage and providing at an output terminal a regulated output voltage, comprising:

a first depletion mode transistor having a control terminal coupled for receiving a first drive signal and a first conduction terminal coupled to the input of the linear regulator circuit;

a second depletion mode transistor having a control terminal coupled for receiving a second drive signal separate from the first drive signal, a first conduction terminal coupled to the output terminal of the linear regulator circuit, and a second conduction terminal coupled to a second conduction terminal of the first depletion mode transistor; and

a control circuit having first and second outputs for providing the first and second drive signals respectively which control the first and second depletion mode transistors to provide the regulated output voltage.

24.   The regulator circuit of claim 23 further including a controller having first and second independently controlled outputs for coupling to the control terminals of the first and second depletion mode transistors.

25.   The regulator circuit of claim 23 wherein the first depletion mode transistor is an n-channel device and the second depletion mode transistor is a p-channel device having a source coupled to the source of the n-channel device.

26. The regulator circuit of claim 23 wherein the first depletion mode transistor is a p-channel device and the second depletion mode transistor is an n-channel device having a source coupled to the source of the p-channel device.

27. (New) An amplifier, comprising:

first and second depletion mode transistors operating in response to first and second signals, respectively, for routing a first current from a first supply terminal to an output of the amplifier; and

third and fourth depletion mode transistors operating in response to the first and second signals for routing a second current from a second supply terminal to the output for summing with the first current to produce an output signal.

28. (New) The amplifier of claim 27, wherein the first depletion mode transistor is an n-channel device having a gate that receives the first signal to control a first conduction path between the first supply terminal and a first node of the amplifier, the second depletion mode transistor is a p-channel device having a gate that receives the second signal to control a conduction path between the first node and the output, the third depletion mode transistor is a p-channel device having a gate that receives the first signal to control a conduction path between the second supply terminal and a second node, and the fourth transistor is an n-channel device having a gate that receives the first signal to control a conduction path between the second node and the output.

29.   (New)   The amplifier of claim 28, wherein the first
transistor has a source coupled to the first node and a drain
coupled to the first supply terminal, the second transistor
has a source coupled to the first node and a drain coupled to
the output, the third transistor has a source coupled to the
second node and a drain coupled to the second supply terminal,
and the fourth transistor has a source coupled to the second
node and a drain coupled to the output.

30.   (New)   The amplifier of claim 29, further comprising a
differential amplifier including:
        a first differential transistor having a gate that
receives the first signal and a drain coupled to the gates of
the third and fourth depletion mode transistors; and
        a second differential transistor having a gate that
receives the second signal, a drain coupled to the gates of
the first and second depletion mode transistors, and a source
coupled to a source of the first differential transistor for
routing a bias current with the first and second signals.

31.   (New)   The amplifier of claim 30, wherein the first and
second differential transistors are depletion mode devices.

32.   (New)   The amplifier of claim 30, further comprising a
fifth depletion mode transistor having a gate and a source
coupled to the second supply terminal and a drain coupled to
the source of the second differential transistor for supplying
the bias current.

33.   (New) An amplifier, comprising:

    a gain stage having first and second inputs for receiving a differential input signal and first and second outputs for providing a differential amplified signal; and

    an output stage including first and second depletion mode transistors operating in response to the differential amplified signal and serially coupled between a supply terminal and an output of the amplifier for providing an output signal.

34.   (New) The amplifier of claim 33, further comprising a feedback path from the output of the amplifier to the first input of the gain stage to reduce the gain of the amplifier.

35.   (New) The amplifier of claim 34, wherein the feedback path includes:

    a first resistor coupled between the output of the amplifier and the first input of the gain stage; and

    a second resistor coupled from the first input of the gain stage to a reference node.

36.   (New) The amplifier of claim 35 for functioning as a voltage regulator, wherein the differential input signal includes a reference voltage applied to the second input of the gain stage to maintain the output signal at a constant potential.

37.   (New) The amplifier of claim 36, wherein a difference between a supply voltage at the supply terminal and the constant potential of the output signal is less than 0.2 volts.

38.   (New)   The amplifier of claim 33, wherein the first depletion mode transistor is a p-channel device having a drain coupled to the supply terminal and a source coupled to a node, and the second depletion mode transistor is an n-channel device having a source coupled to the node and a drain coupled to the output of the amplifier.

39.   (New)   The amplifier of claim 33, further comprising a level shift circuit having first and second inputs for level shifting the differential amplified signal by a predefined potential to provide a differential level shifted signal at first and second outputs of the level shift circuit.

<u>REMARKS</u>

Claims 23-39 are pending in this application. Claims 27-39 are added by this preliminary amendment. Applicants respectfully request that this preliminary amendment be entered prior to examination of Application No. 09/580,560.

As a convenience to the examiner, a copy of the specification, drawings and claims is attached to this amendment to present a clean copy of the continuation-in-part application after inclusion of matter in this amendment.
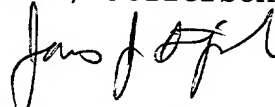
CONCLUSION

Applicants respectfully request consideration and allowance of claims 23-39.

A continuation-in-part application fee in the amount of $740.00 is believed due, the Commissioner is hereby authorized to charge any fees or credit any overpayment to Deposit Account 501086.

If there are matters which can be discussed by telephone to further the prosecution of this application, applicants invite the examiner to call the undersigned attorney/agent at the examiner's convenience.

Respectfully submitted,
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